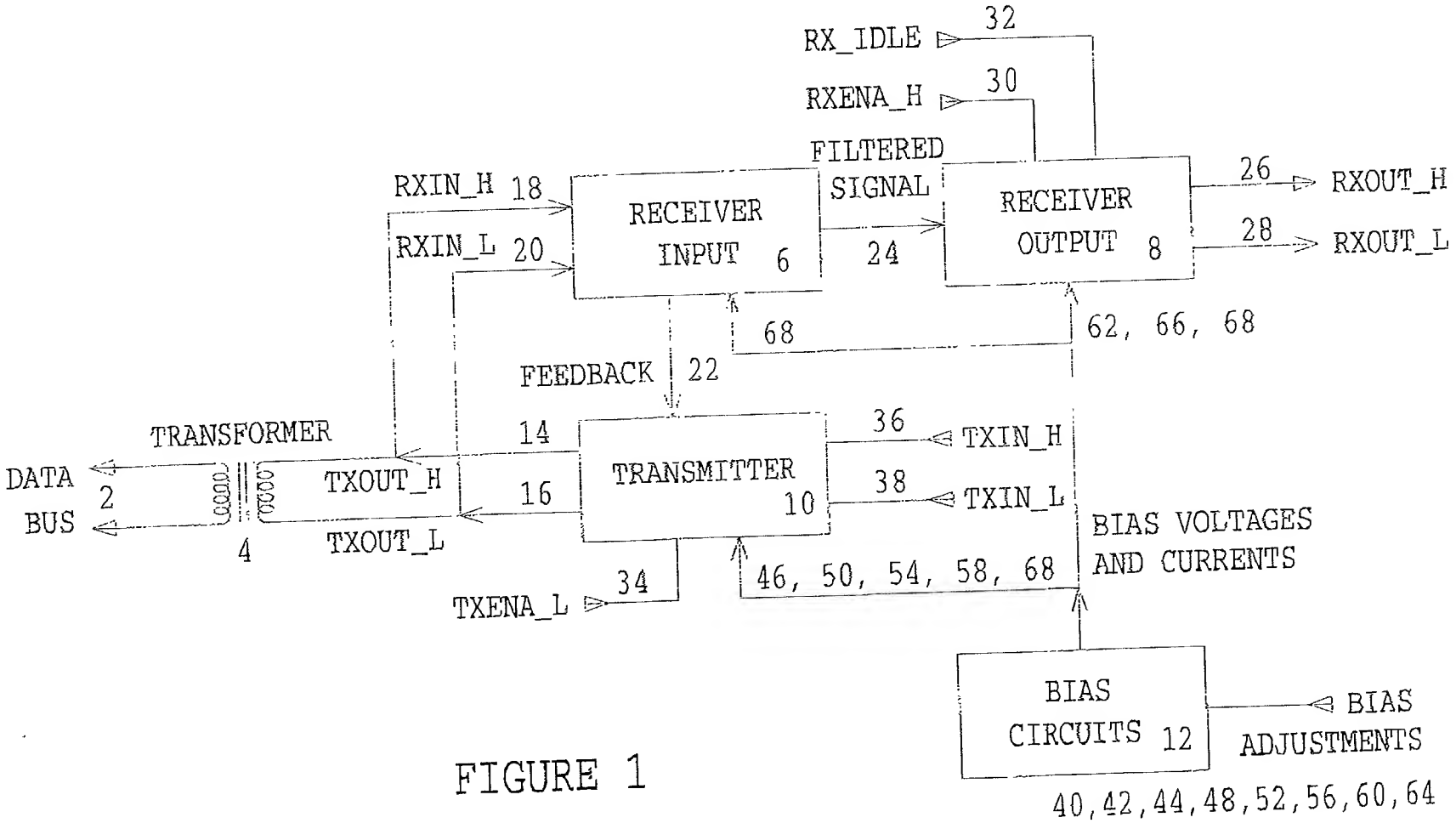

FIGURE 1

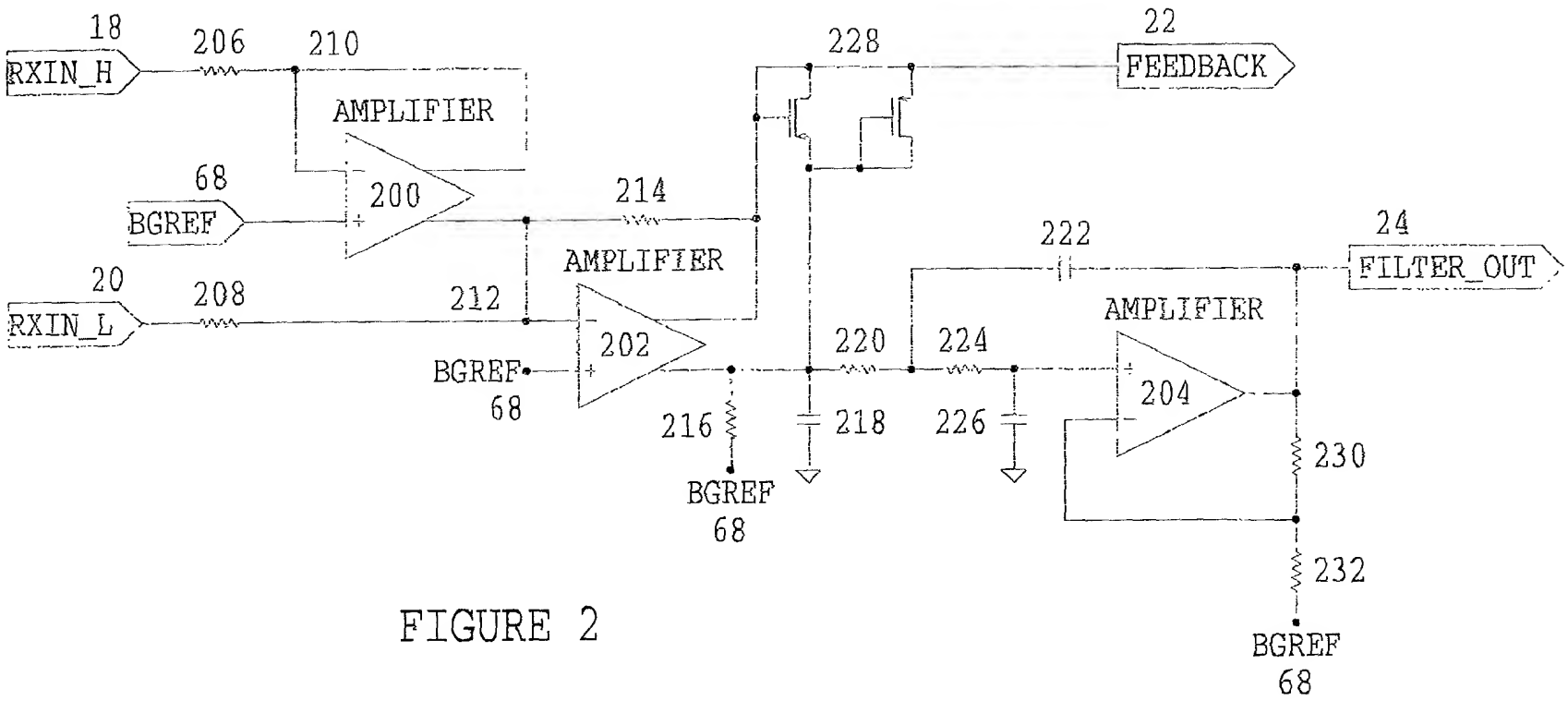
18
RXIN_H
206
210
AMPLIFIER
200
68
BGREF
214
228
22
FEEDBACK
20
RXIN_L
208
212
AMPLIFIER
202
BGREF
68
216
BGREF
68
220
218
224
226
222
24
FILTER_OUT
AMPLIFIER
204
230
232
BGREF
68

FIGURE 2

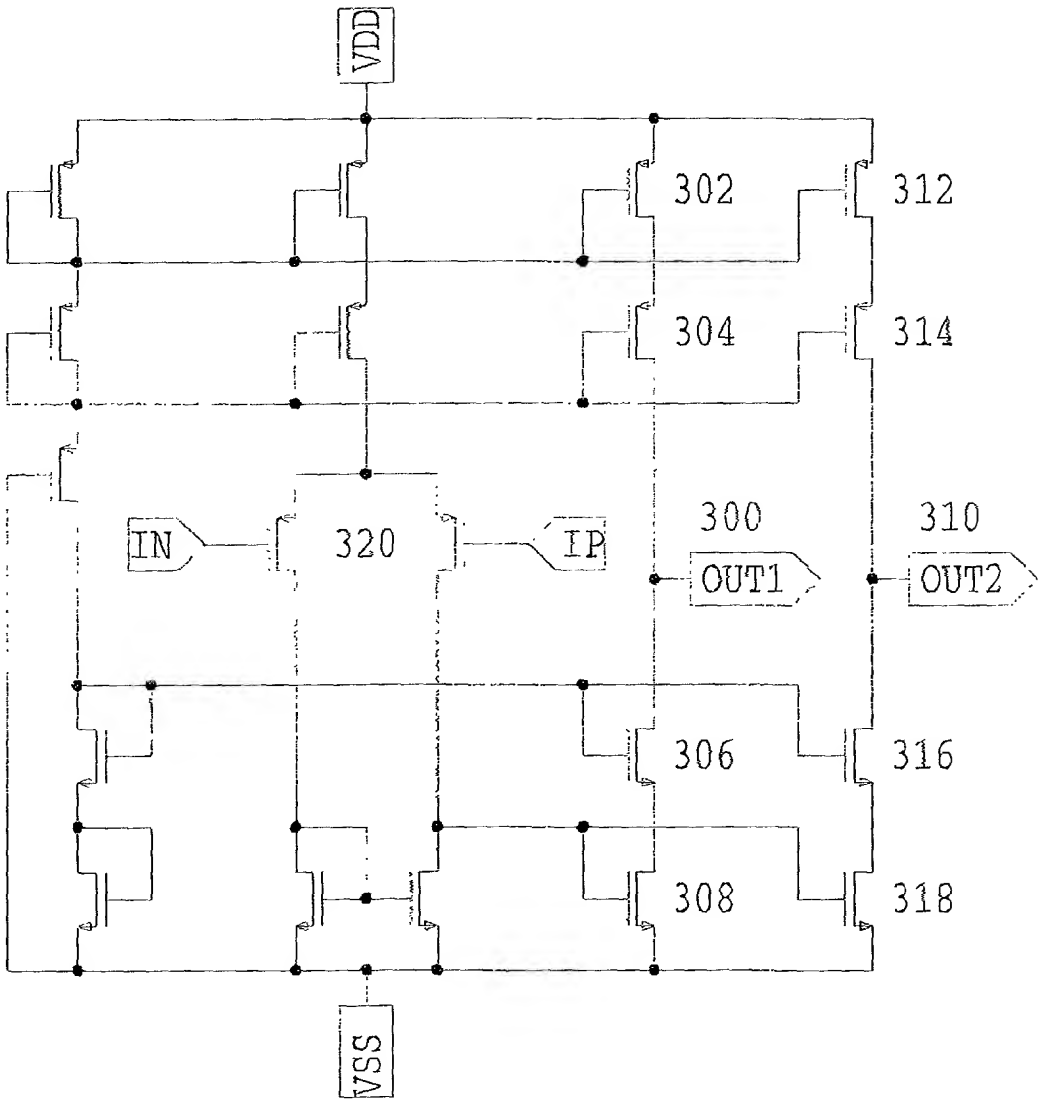

FIGURE 3

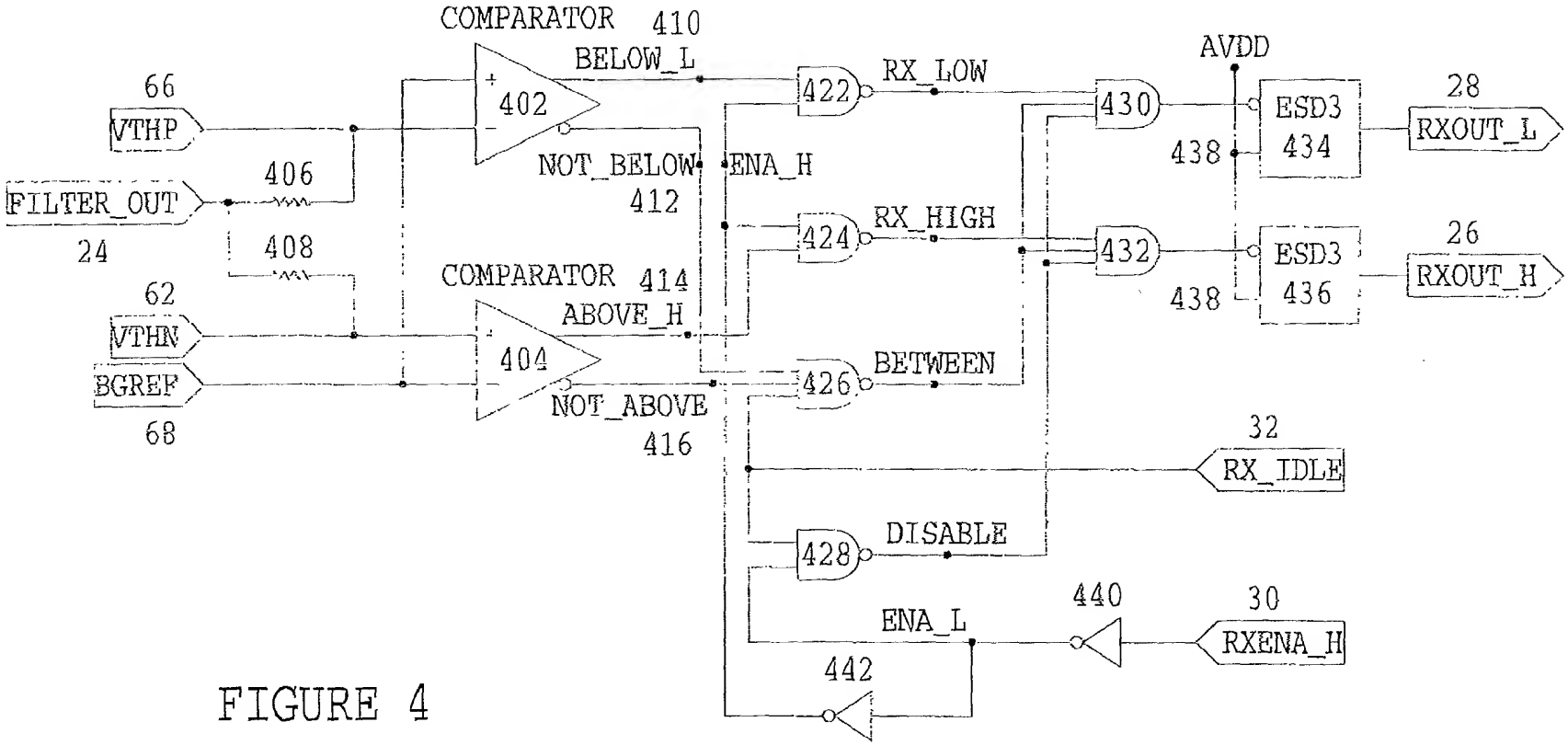

FIGURE 4

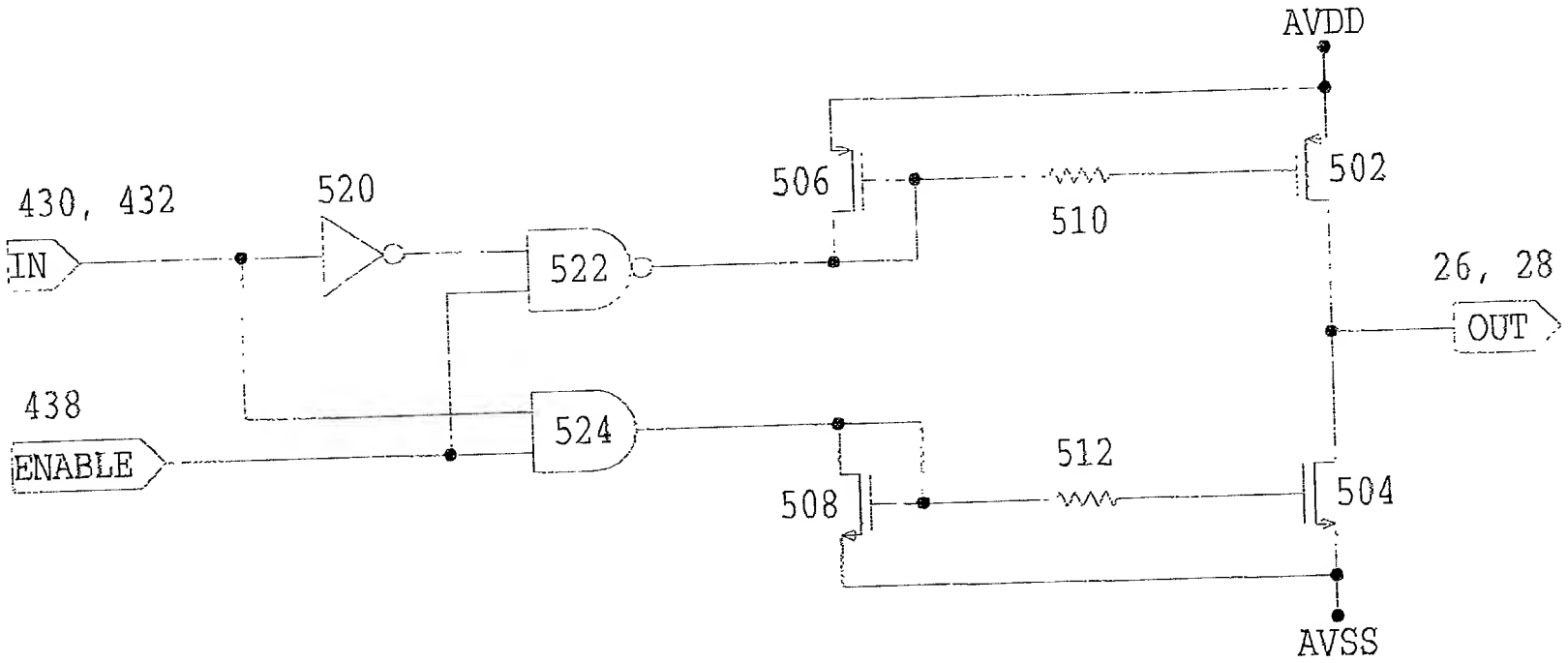
AVDD
430, 432
IN
520
522
506
510
502
26, 28
OUT
438
ENABLE
524
512
508
504
AVSS

FIGURE 5

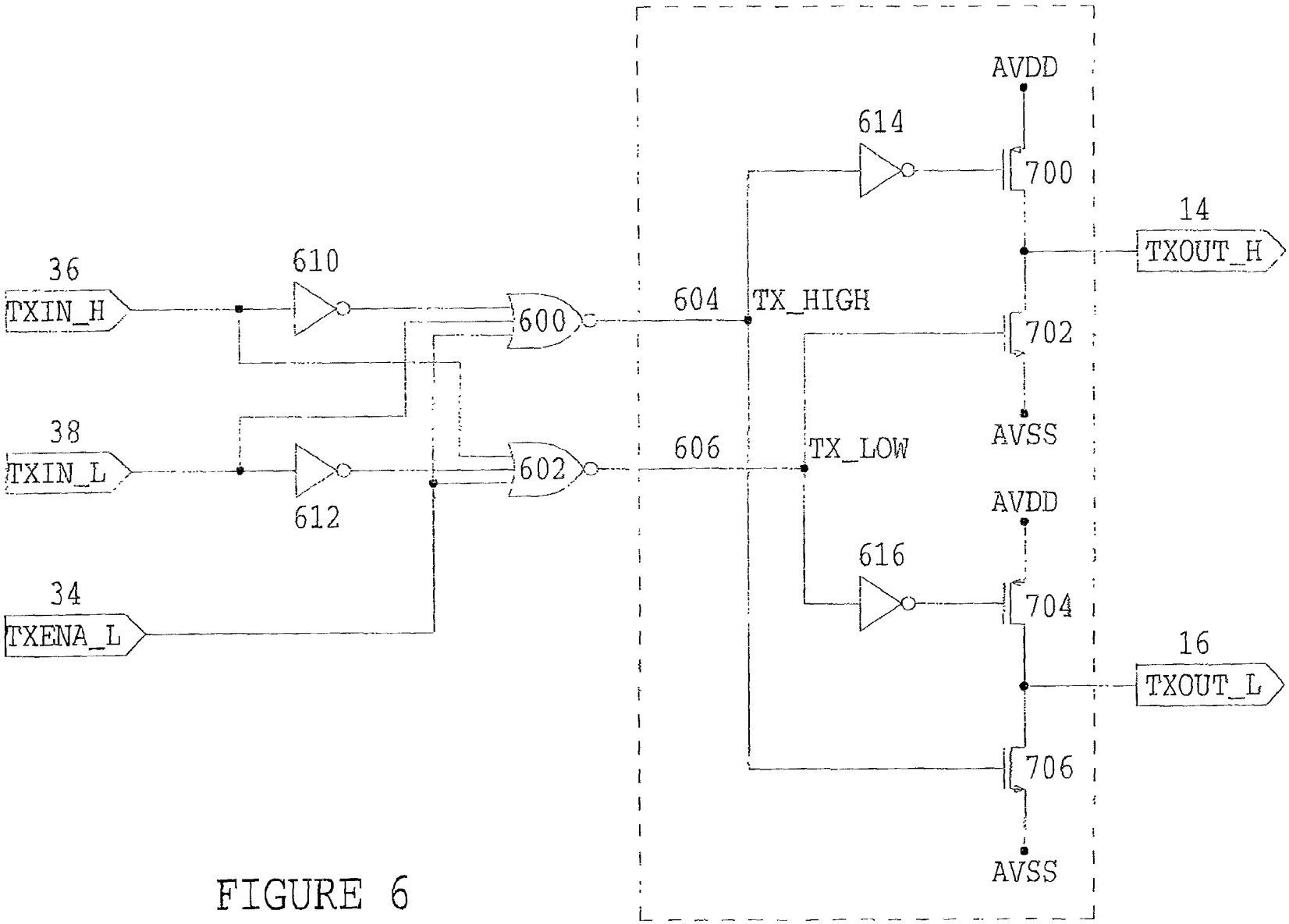
AVDD
614
700
14
TXOUT_H
36
TXIN_H
610
600
604
TX_HIGH
702
AVSS
38
TXIN_L
612
602
606
TX_LOW
AVDD
616
704
34
TXENA_L
16
TXOUT_L
706
AVSS

FIGURE 6

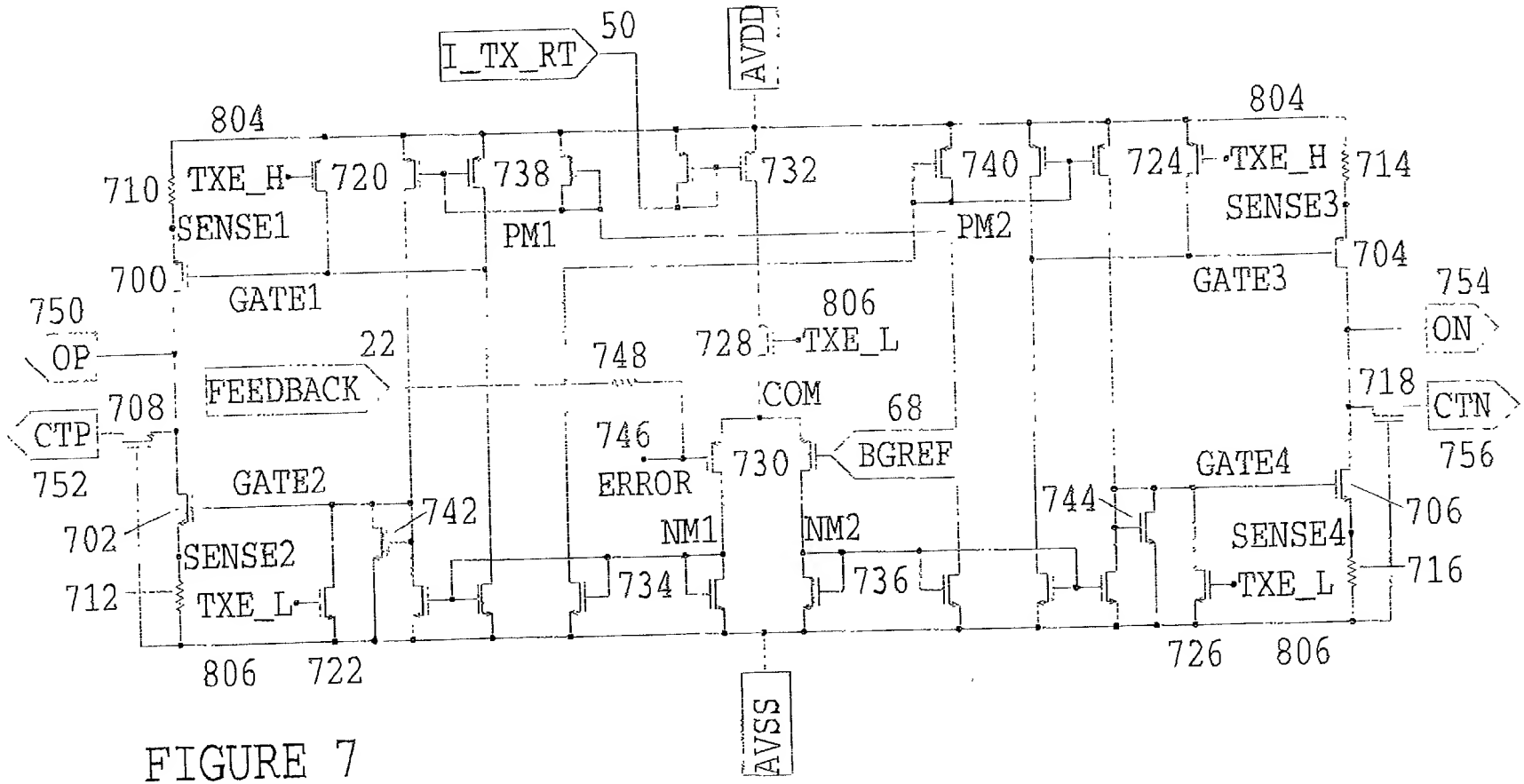
I_TX_RT
50
AVDD
804
804
710
TXE_H
720
738
732
740
724
TXE_H
714
SENSE1
PM1
PM2
SENSE3
700
GATE1
704
GATE3
754
750
806
ON
OP
22
728
TXE_L
748
718
FEEDBACK
COM
CTN
708
68
CTP
746
730
BGREF
756
752
GATE2
GATE4
744
706
702
742
NM1
NM2
SENSE4
SENSE2
734
736
716
712
TXE_L
TXE_L
806
722
726
806
AVSS

FIGURE 7

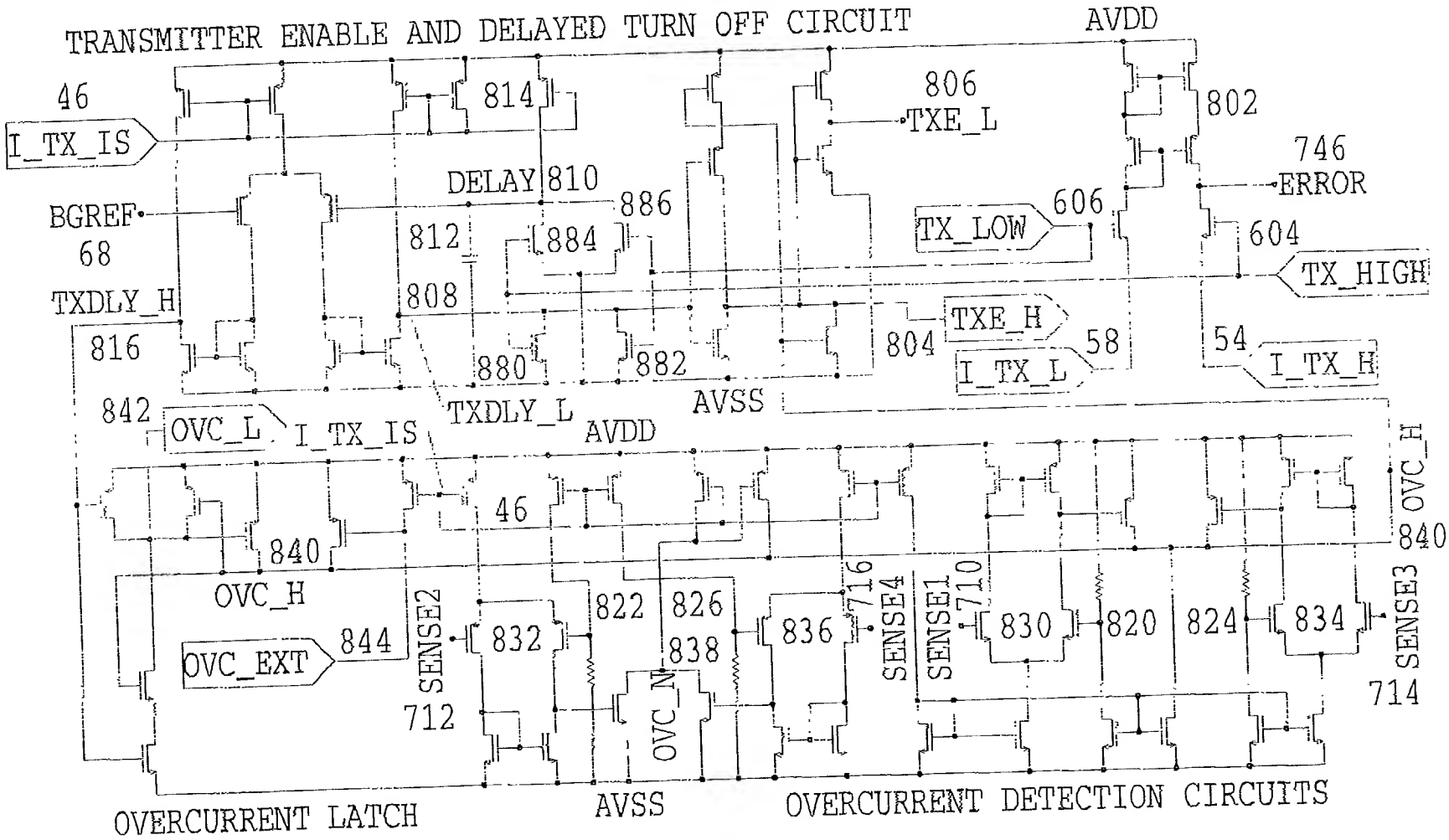
TRANSMITTER ENABLE AND DELAYED TURN OFF CIRCUIT
AVDD
46
I_TX_IS
814
806
TXE_L
802
746
ERROR
DELAY
810
886
BGREF
68
812
884
606
TX_LOW
604
TX_HIGH
TXDLY_H
808
816
880
882
804
TXE_H
58
I_TX_L
54
I_TX_H
AVSS
842
OVC_L
I_TX_IS
TXDLY_L
AVDD
OVC_H
840
46
840
OVC_H
822
826
716
710
830
820
824
834
SENSE3
714
844
832
836
838
SENSE4
SENSE1
OVC_EXT
SENSE2
712
OVC_N
OVERCURRENT LATCH
AVSS
OVERCURRENT DETECTION CIRCUITS

FIGURE 8

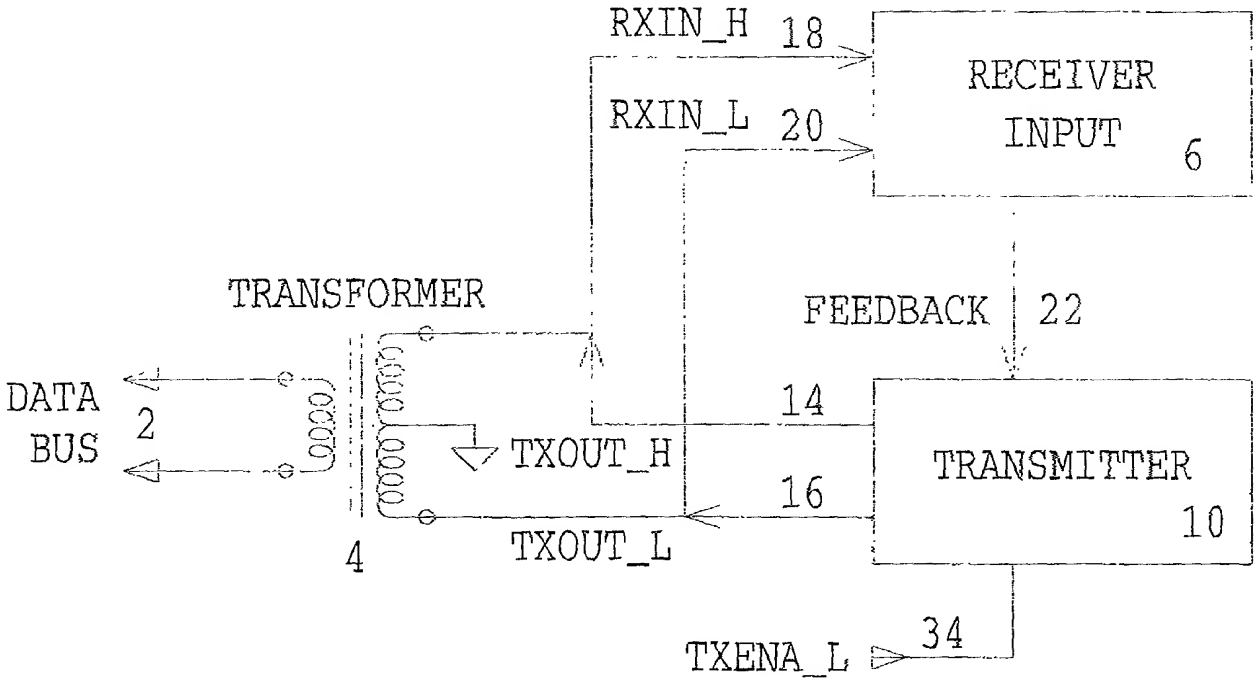

FIGURE 9

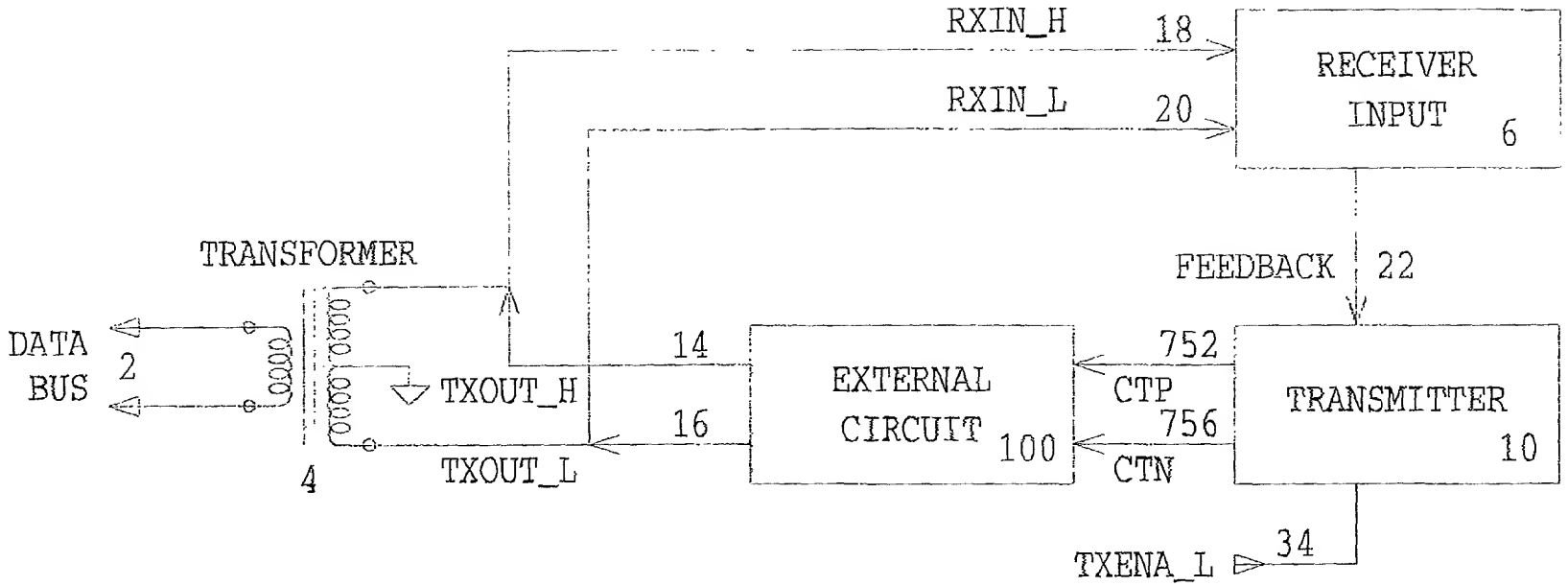
RXIN_H
18
RECEIVER
INPUT
6
RXIN_L
20
TRANSFORMER
FEEDBACK
22
DATA
BUS
2
14
752
EXTERNAL
CIRCUIT
100
CTP
TRANSMITTER
10
TXOUT_H
16
756
CTN
4
TXOUT_L
34
TXENA_L

FIGURE 10

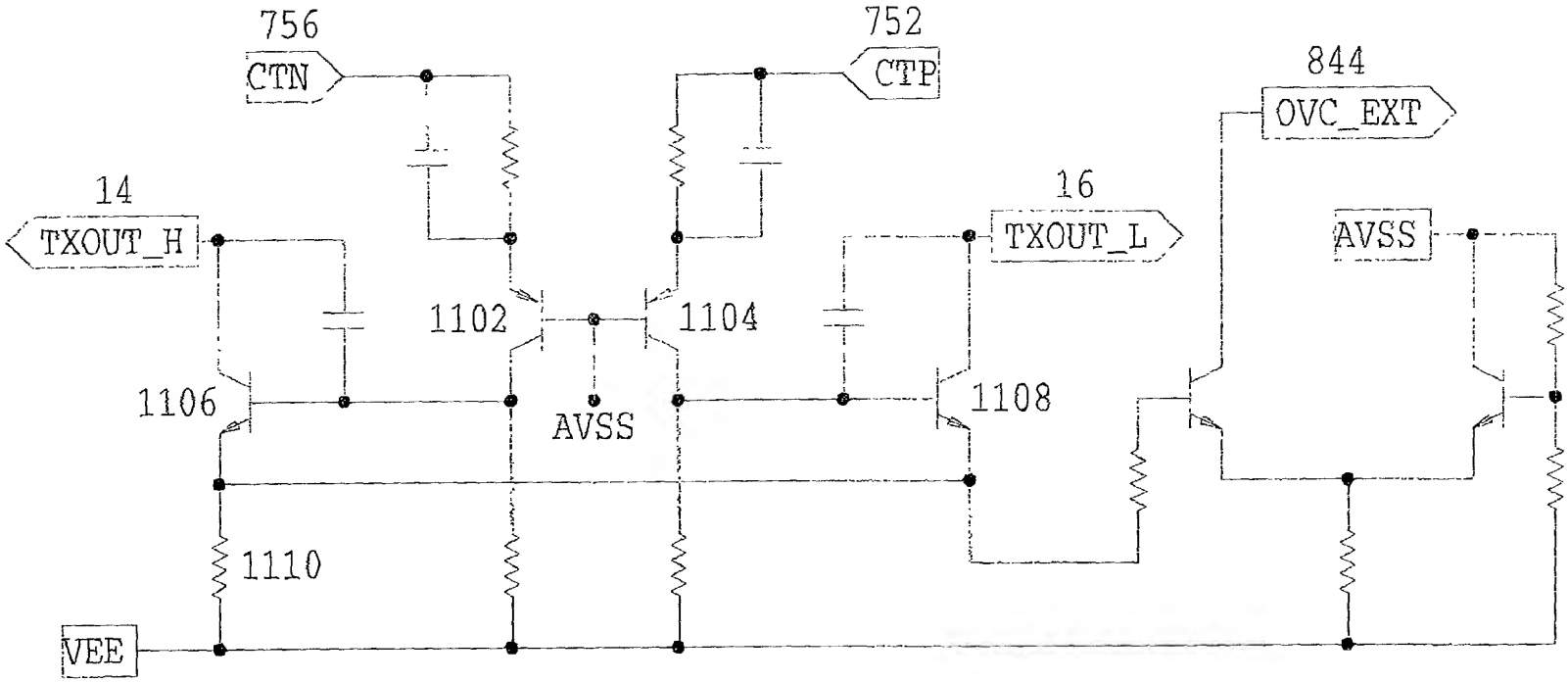

FIGURE 11

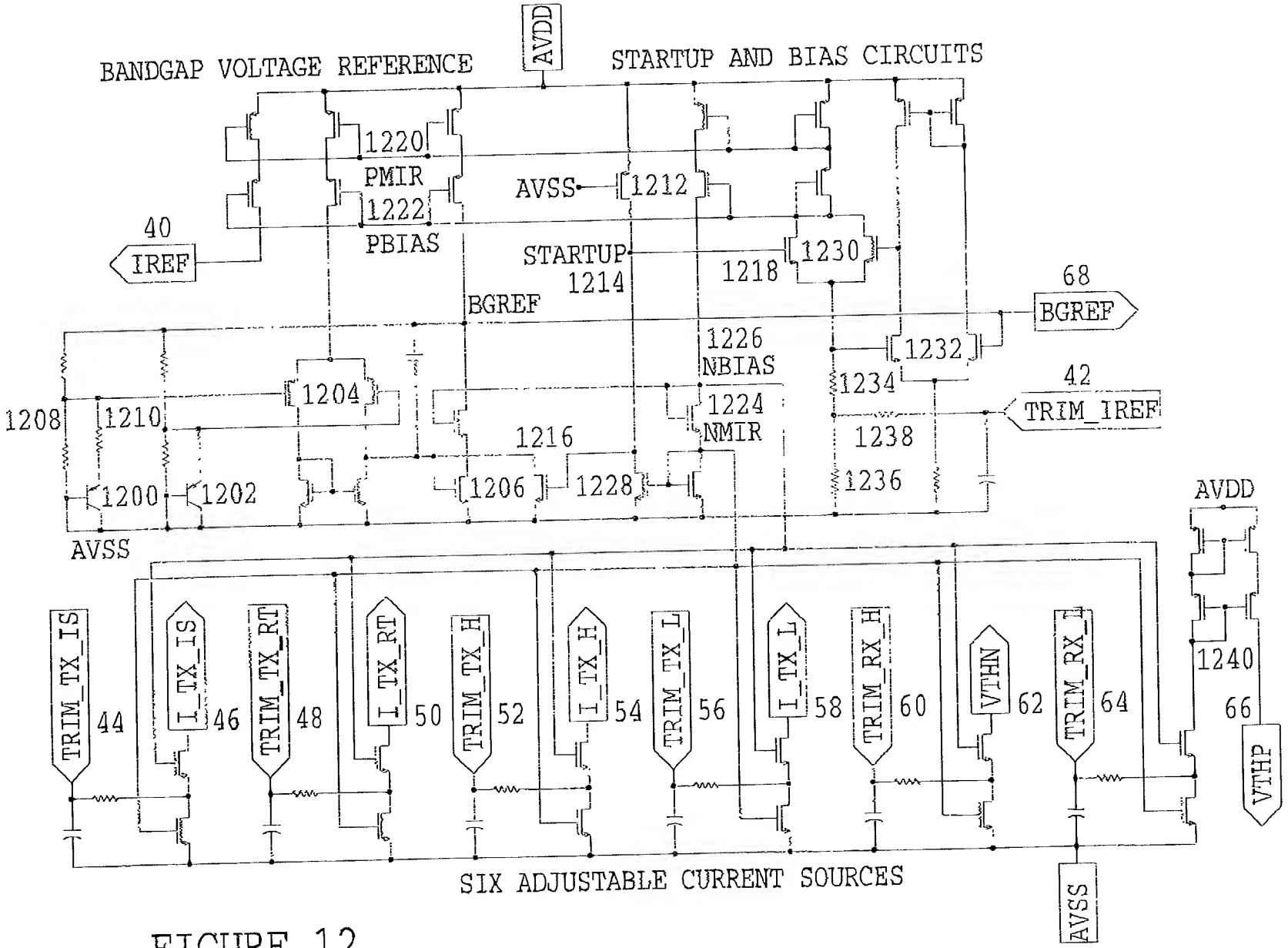
BANDGAP VOLTAGE REFERENCE
AVDD
STARTUP AND BIAS CIRCUITS
1220
PMIR
1222
PBIAS
AVSS
1212
40
IREF
STARTUP
1214
1218
1230
68
BGREF
BGREF
1226
NBIAS
1232
1234
42
TRIM_IREF
1204
1208
1210
1224
NMIR
1216
1238
1206
1228
1236
1200
1202
AVSS
AVDD
TRIM_TX_IS
44
I_TX_IS
46
TRIM_TX_RT
48
I_TX_RT
50
TRIM_TX_H
52
I_TX_H
54
TRIM_TX_L
56
I_TX_L
58
TRIM_RX_H
60
VTHN
62
TRIM_RX_L
64
1240
66
VTHP
SIX ADJUSTABLE CURRENT SOURCES
AVSS

FIGURE 12